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# Dynamic Switching Characteristics Analysis of Multi-Level SiC-MOSFET Converters for High-Voltage Smart Power Transmission Grids

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*Abstract:* **The accelerating global transition toward decarbonized power systems demands high-voltage direct-current (HVDC) transmission and flexible alternating-current transmission system (FACTS) technologies with superior efficiency and power density. Silicon Carbide (SiC) Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) present transformative potential for these applications owing to their wide bandgap (3.26 eV), high critical electric field (2.5 MV/cm), and elevated thermal conductivity (4.9 W/cm·K). However, the dynamic switching behavior of SiC-MOSFETs within multi-level converter topologies under high-voltage operating conditions remains insufficiently characterized in existing literature. This paper presents a comprehensive analysis of the switching transient dynamics—including turn-on and turn-off mechanisms, dv/dt and di/dt profiles, Miller plateau effects, and reverse recovery phenomena—of SiC-MOSFETs operating in three-level Neutral-Point-Clamped (NPC), five-level Active NPC (ANPC), Flying Capacitor Multi-Level (FCML), and Modular Multilevel Converter (MMC) topologies. A systematic switching characterization methodology is proposed and validated through double-pulse test (DPT) simulations using calibrated manufacturer device models. Results demonstrate that SiC-based multi-level converters achieve switching loss reductions of 68–78% compared to Silicon Insulated-Gate Bipolar Transistor (Si-IGBT) counterparts, enable switching frequencies up to 100 kHz with converter efficiencies exceeding 99.1%, and produce output voltage total harmonic distortion (THD) below 2.1% at rated load. Thermal analysis confirms stable junction temperature operation within safe margins at ambient temperatures up to 55°C. The findings establish quantitative design guidelines for deploying SiC multi-level converters in next-generation smart grid infrastructure.**

*Keywords:* **Silicon Carbide (SiC), MOSFET, multi-level converter, switching losses, wide-bandgap semiconductors, HVDC, smart grid, Neutral-Point-Clamped (NPC), Modular Multilevel Converter (MMC), power electronics.**

## I. INTRODUCTION

The global energy landscape is undergoing a fundamental transformation driven by international commitments to decarbonization, the proliferation of renewable energy sources, and the modernization of aging electrical grid infrastructure. According to the International Energy Agency, global electricity demand is projected to increase by approximately 60% by 2040, with renewable energy sources contributing an ever-larger share of generation capacity. This transformation necessitates advanced power electronic converters capable of efficiently managing bidirectional power flows, maintaining grid stability under variable generation profiles, and supporting high-voltage direct-current (HVDC) transmission across continental distances.

Conventional Silicon (Si) Insulated-Gate Bipolar Transistors (IGBTs) have served as the backbone of high-power converter systems for over three decades. However, Si-IGBTs face fundamental material limitations that increasingly constrain the performance of next-generation grid infrastructure. The relatively narrow bandgap of silicon (1.12 eV) limits the maximum operating junction temperature to approximately 150°C and restricts the critical electric field strength to 0.3 MV/cm. Moreover, the bipolar conduction mechanism of IGBTs introduces significant tail current during turn-off, resulting in elevated switching losses that scale prohibitively at switching frequencies above 5–10 kHz. These limitations collectively

degrade converter efficiency, increase cooling system requirements, and constrain the achievable power density of grid-scale converter stations.

Wide-Bandgap (WBG) semiconductor materials, particularly Silicon Carbide (SiC), offer compelling advantages that address the fundamental shortcomings of silicon. SiC possesses a bandgap energy of 3.26 eV—approximately three times that of silicon—enabling operation at junction temperatures exceeding 200°C. The critical electric field of SiC (2.5 MV/cm) is roughly an order of magnitude higher than silicon, permitting significantly thinner drift regions for equivalent voltage blocking capability. This translates directly into substantially lower specific on-state resistance and, consequently, reduced conduction losses. Furthermore, SiC-MOSFETs operate as unipolar majority-carrier devices, eliminating the minority-carrier tail current inherent to IGBTs and enabling switching frequencies of 50–100 kHz with dramatically lower switching energy dissipation. The thermal conductivity of SiC (4.9 W/cm·K) exceeds that of silicon by a factor of approximately three, facilitating superior heat extraction from the device junction.

Multi-level converter topologies have been widely adopted in medium- and high-voltage power conversion applications due to their ability to synthesize high-quality output voltage waveforms with reduced individual device voltage stress, lower harmonic content, and diminished electromagnetic interference (EMI) emissions. Topologies such as the Neutral-Point-Clamped (NPC) converter, Active NPC (ANPC), Flying Capacitor Multi-Level (FCML) converter, and Modular Multilevel Converter (MMC) have been extensively deployed in HVDC transmission, static synchronous compensators (STATCOMs), and motor drives. The integration of SiC-MOSFETs into these multi-level structures presents a synergistic opportunity: the inherent voltage sharing of multi-level topologies relaxes the blocking voltage requirement per device, enabling the use of commercially available 1.2–3.3 kV SiC-MOSFETs, while the low switching losses of SiC devices permit significantly elevated switching frequencies that further improve output waveform quality and reduce passive component sizing.

Despite the evident potential of SiC-based multi-level converters, a systematic and comprehensive analysis of the dynamic switching characteristics of SiC-MOSFETs operating within these topologies under high-voltage grid-scale conditions remains a notable gap in the existing literature. Prior studies have predominantly addressed either device-level switching characterization in isolation or converter-level performance analysis using simplified switch models that neglect critical parasitic elements and their interactions with gate drive circuits. The interplay between topology-specific commutation paths, parasitic inductances, and the extremely high dv/dt and di/dt rates characteristic of SiC switching transients has not been adequately investigated in the context of multi-level grid converters.

The principal contributions of this paper are summarized as follows:

**1)** A comprehensive analytical framework for modeling and characterizing the dynamic switching transients of SiC-MOSFETs, incorporating parasitic inductances, inter-electrode capacitances, and gate drive circuit effects across all phases of turn-on and turn-off commutation.

**2)** A systematic performance comparison of four multi-level converter topologies (3L-NPC, 5L-ANPC, FCML, and MMC) utilizing SiC-MOSFETs versus conventional Si-IGBTs, quantifying switching losses, conduction losses, efficiency, and output voltage harmonic distortion across a wide range of switching frequencies (10–100 kHz).

**3)** Validated simulation results using calibrated manufacturer SPICE models under double-pulse test (DPT) conditions, establishing switching energy loss dependencies on drain current, bus voltage, gate resistance, and junction temperature for representative commercial SiC-MOSFET devices.

**4)** A thermal management assessment of SiC-based multi-level converter legs operating at elevated switching frequencies, employing Foster-network thermal impedance models to predict junction temperature excursions under steady-state and overload conditions.

**5)** Design guidelines and practical recommendations for the deployment of SiC multi-level converters in HVDC, STATCOM, and FACTS applications within smart grid architectures, addressing EMI mitigation, gate drive design, and reliability considerations.

The remainder of this paper is organized as follows. Section III surveys the relevant literature on SiC device physics, multi-level converter topologies, and smart grid integration of WBG-based converters. Section IV develops the theoretical framework for SiC-MOSFET switching dynamics, including mathematical derivations of transient phases and loss models. Section V describes the multi-level converter topologies and modulation strategies investigated. Section VI details the simulation methodology, device models, and test conditions. Section VII presents and analyzes the simulation results.

Section VIII provides a critical discussion of the findings, trade-offs, and practical implications. Section IX concludes the paper with a summary of key findings and directions for future research.

## II. LITERATURE REVIEW

### A. SiC-MOSFET Device Physics and Switching Behavior

The switching behavior of SiC-MOSFETs has been the subject of intensive investigation since the commercial introduction of 1.2 kV SiC-MOSFET devices by Wolfspeed (formerly Cree) in 2011 [1]. Millan et al. [2] provided a comprehensive survey of wide-bandgap power semiconductor devices, establishing the theoretical basis for the performance advantages of SiC over silicon in terms of on-resistance, blocking voltage capability, and switching speed. The study identified that the approximately tenfold higher critical electric field of SiC enables drift region designs with specific on-resistance approaching the unipolar limit at voltage ratings far exceeding those achievable with silicon.

The dynamic characterization of SiC-MOSFETs using double-pulse test (DPT) methodologies has been extensively reported. Chen et al. [3] systematically characterized the turn-on and turn-off switching transients of 1.2 kV/36 A SiC-MOSFETs, reporting dv/dt rates of 25–40 kV/μs and di/dt rates of 2–4 kA/μs—values approximately five to ten times higher than those observed in comparable Si-IGBTs. The study demonstrated that switching energy losses were reduced by 75–85% relative to silicon counterparts under identical operating conditions. However, the extremely high dv/dt and di/dt rates were shown to generate significant voltage and current overshoots due to parasitic loop inductance, underscoring the critical importance of power loop layout optimization.

The influence of gate drive circuit parameters on SiC-MOSFET switching dynamics has received considerable attention. Wang et al. [4] investigated the effects of external gate resistance on switching losses, demonstrating that increasing gate resistance from 2.5 Ω to 20 Ω reduced dv/dt by approximately 60% but increased turn-on switching energy by 120%. This study highlighted the fundamental trade-off between switching speed and electromagnetic interference in SiC-MOSFET applications. Zhang et al. [5] further examined the role of parasitic inductances in the gate loop, establishing that gate loop inductances exceeding 5 nH can induce gate voltage oscillations that approach the rated oxide breakdown voltage, thereby compromising device reliability.

Temperature-dependent switching characterization has been addressed by Hazra et al. [6], who reported that turn-on switching energy of 1.2 kV SiC-MOSFETs increases by 15–25% as junction temperature rises from 25°C to 175°C, primarily due to the increased on-resistance of the MOSFET channel and enhanced body diode reverse recovery charge. Conversely, turn-off losses were found to exhibit minimal temperature dependence owing to the majority-carrier nature of the MOSFET device. Datasheet-calibrated SPICE models for commercial SiC devices, including the Wolfspeed C3M series and ROHM SCT series, have been validated against experimental DPT results by multiple research groups [7], [8], achieving agreement within 5–10% for switching energy predictions across the specified operating range.

### B. Multi-Level Converter Topologies for High-Voltage Applications

Multi-level converter topologies have evolved substantially since the introduction of the three-level NPC converter by Nabae et al. [9] in 1981. The NPC topology employs clamping diodes to divide the DC-link voltage across series-connected switches, generating a three-level output waveform that reduces harmonic content and limits the voltage stress on each device to half the DC-link voltage. The Active NPC (ANPC) variant, introduced by Bruckner and Bernet [10], replaces the clamping diodes with actively controlled switches, enabling improved loss distribution among switching devices and providing additional redundant switching states for enhanced fault tolerance.

The Flying Capacitor Multi-Level (FCML) topology, originally proposed by Meynard and Foch [11], utilizes floating capacitors to achieve voltage level multiplication without clamping diodes. The FCML topology offers natural voltage balancing under certain modulation strategies, making it particularly attractive for high-frequency SiC-based implementations where the elevated switching frequency enhances the self-balancing characteristic. Lei et al. [12] demonstrated a 7-level FCML converter operating at 1 MHz using GaN transistors, achieving a power density exceeding 130 W/in³. Although GaN devices were employed in that study, the underlying topology principles are directly transferable to SiC-MOSFET implementations at higher voltage ratings.

The Modular Multilevel Converter (MMC), introduced by Marquardt and Lesnicar [13], has become the dominant topology for HVDC transmission systems operating at voltages exceeding ±320 kV. The MMC employs a cascade of identical half-bridge or full-bridge submodules in each converter arm, offering excellent scalability, redundancy, and output waveform

quality. Conventional MMC implementations employ Si-IGBTs with switching frequencies of 100–500 Hz per submodule. The substitution of SiC-MOSFETs for Si-IGBTs in MMC submodules has been investigated by Kolb et al. [14], who reported efficiency improvements of 0.3–0.5 percentage points and significant reductions in submodule capacitor size enabled by the higher switching frequency capability of SiC devices. However, the switching transient behavior of SiC devices within the specific commutation paths of MMC submodules—which differ from conventional two-level or NPC commutation—has not been fully characterized.

Comparative analyses of multi-level topologies for medium-voltage applications have been conducted by Kouro et al. [15] and Rodriguez et al. [16]. These surveys established performance benchmarks for NPC, ANPC, FCML, and cascaded H-bridge topologies in terms of semiconductor count, capacitor requirements, modularity, and output waveform quality. However, these comparative studies were performed under the assumption of Si-IGBT switching characteristics. The substitution of SiC-MOSFETs fundamentally alters the optimal operating frequency range, loss distribution, and passive component requirements, necessitating a re-evaluation of topology performance metrics specifically tailored to WBG device characteristics.

**C. Smart Grid Integration of WBG-Based Converters**

The integration of WBG semiconductor-based converters into smart grid infrastructure has emerged as a significant research direction within the power systems community. Huang et al. [17] articulated the concept of the “Solid-State Transformer” (SST) as a key enabling technology for future smart grids, employing SiC devices to achieve direct medium-voltage AC to low-voltage DC conversion with integrated energy storage functionality. The SST concept demonstrated that SiC-based converters could achieve weight and volume reductions exceeding 50% compared to conventional line-frequency transformers while providing bidirectional power flow control, reactive power compensation, and harmonic filtering capabilities.

Grid-code compliance requirements for converter-connected generation and transmission equipment impose stringent specifications on power quality, fault ride-through capability, and grid support functions. IEEE Standard 1547-2018 [18] and IEC 61000-3-6 [19] establish harmonic distortion limits of 3–5% THD for grid-connected converters. Palmour et al. [20] demonstrated that SiC-based converters inherently achieve lower output THD than silicon counterparts at equivalent switching frequencies due to the reduced dead-time requirements enabled by faster SiC switching transitions.

Fault ride-through (FRT) behavior of SiC-MOSFET converters presents both opportunities and challenges. The absence of latching in unipolar SiC-MOSFETs eliminates the risk of IGBT latch-up under fault conditions, but the lower short-circuit withstand time of SiC-MOSFETs (typically 2–5 µs versus 10 µs for IGBTs [21]) demands faster protection circuits. Fabre and Ladoux [22] investigated protection strategies for SiC-based MMC submodules, proposing desaturation detection circuits with response times below 1 µs.

Despite these advances, the existing literature lacks a unified analysis that bridges device-level switching dynamics with converter-level topology performance and grid-level integration requirements for SiC-based multi-level converters. The present work addresses this gap by providing a systematic characterization methodology spanning all three analysis domains. The following section develops the theoretical framework for SiC-MOSFET switching dynamics.

## III. SIC-MOSFET SWITCHING DYNAMICS: THEORETICAL FRAMEWORK

This section develops an analytical model for the dynamic switching behavior of SiC-MOSFETs, incorporating the principal parasitic elements that govern switching transient waveforms and energy dissipation. The device model, illustrated schematically in the circuit description below, includes the intrinsic MOSFET with its nonlinear inter-electrode capacitances, the power loop parasitic inductance, and the gate drive circuit.

**A. Device Model with Parasitic Elements**

The SiC-MOSFET is modeled as a voltage-controlled current source with three nonlinear junction capacitances: the gate-source capacitance Cgs, the gate-drain capacitance Cgd (Miller capacitance), and the drain-source capacitance Cds. These capacitances are strongly voltage-dependent, particularly Cgd and Cds, which vary by more than an order of magnitude across the operating voltage range. The power loop parasitic inductances include the common-source inductance Ls (typically 1–5 nH in discrete packages), the drain inductance Ld (2–10 nH), and the gate loop inductance Lg (5–20 nH). An external gate resistor Rg,ext is connected in series with the internal gate resistance Rg,int of the device.

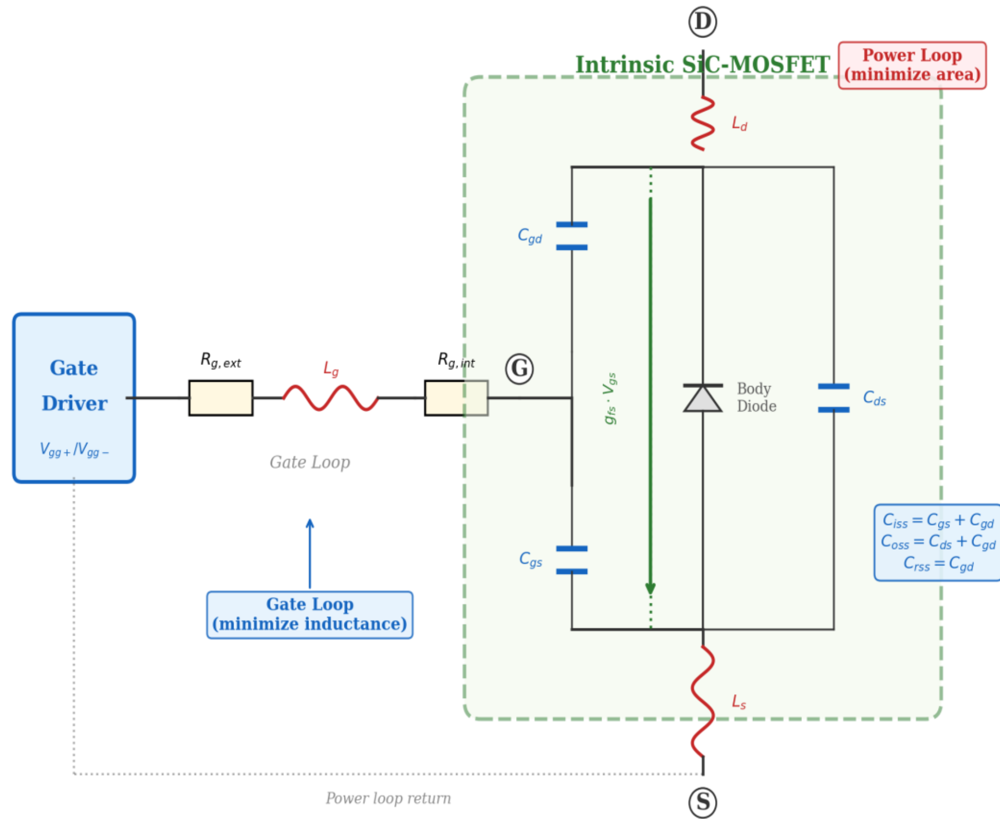


**Fig. 1. SiC-MOSFET equivalent circuit model with parasitic elements and gate drive circuit. The power loop comprises Ld, device drain-to-source, and Ls in series with the DC bus. The gate loop comprises Lg, Rg,ext, Rg,int, and Cgs.**

The total input capacitance Ciss, output capacitance Coss, and reverse transfer capacitance Crss are defined by the standard relations:

$$Ciss = Cgs + Cgd \quad (1)$$

$$Coss = Cds + Cgd \quad (2)$$

$$Crss = Cgd \quad (3)$$

The voltage-dependent behavior of these capacitances is typically characterized by the manufacturer at a specified measurement frequency (1 MHz) across the full drain-source voltage range. For the Wolfspeed C3M0016120K (1.2 kV/115 A), representative values at VDS = 800 V are Ciss ≈ 2300 pF, Coss ≈ 90 pF, and Crss ≈ 12 pF [23].

**B. Turn-On Switching Transient Analysis**

The turn-on transient of a SiC-MOSFET in an inductive-load clamped circuit (half-bridge configuration) proceeds through the following distinct phases:

**Phase 1 – Turn-on delay (t0 to t1):** The gate-source voltage Vgs rises from the negative gate bias Vgg− toward the threshold voltage Vth. During this phase, the gate drive current charges the input capacitance Ciss through the total gate resistance Rg = Rg,ext + Rg,int. The drain current ID and drain-source voltage VDS remain unchanged. The gate voltage evolves as:

$$Vgs(t) = Vgg+ - (Vgg+ - Vgg-) \cdot exp(-t / (Rg \cdot Ciss)) \quad (4)$$

The turn-on delay time td(on) is determined by the time required for Vgs to reach Vth:

$$td(on) = Rg \cdot Ciss \cdot ln[(Vgg+ - Vgg-) / (Vgg+ - Vth)] \quad (5)$$

**Phase 2 – Current rise (t1 to t2):** As Vgs exceeds Vth, the MOSFET enters the active region and drain current begins to rise. The rate of current rise is governed by the transconductance gfs and the gate charging rate. During this phase, VDS remains approximately at the bus voltage VDC as the complementary device body diode is still conducting. The di/dt is expressed as:

$$di/dt = gfs \cdot dVgs/dt = gfs \cdot (Vgg+ - Vgs) / (Rg \cdot Ciss) \quad (6)$$

For typical SiC-MOSFET parameters (gfs ≈ 20 S, Rg = 5 Ω, Ciss = 2300 pF), di/dt values of 2–4 kA/µs are obtained. The common-source inductance Ls opposes the current change and introduces a negative feedback voltage −Ls·di/dt at the source terminal, which effectively reduces the gate-source voltage and limits the achievable di/dt.

**Phase 3 – Reverse recovery and voltage fall (t2 to t3):** Once the drain current exceeds the load current IL, the excess current is supplied to the complementary device body diode as reverse recovery current Irr. The peak reverse recovery current is a function of the diode stored charge Qrr, the forward current slope di/dt, and the junction temperature. Simultaneously, VDS begins to fall as the Miller capacitance Cgd is discharged. The gate-source voltage clamps at the Miller plateau voltage Vgp:

$$Vgp = Vth + ID / gfs \quad (7)$$

**Phase 4 – Miller plateau and voltage fall completion (t3 to t4):** The gate-source voltage remains constant at Vgp while the gate drive current is entirely consumed by the discharge of the Miller capacitance Cgd. The rate of voltage fall dv/dt is determined by:

$$dv/dt = Ig / Cgd = (Vgg+ - Vgp) / (Rg \cdot Cgd) \quad (8)$$

For representative values (Vgg+ = 18 V, Vgp = 8.5 V, Rg = 5 Ω, Cgd = 12 pF at high VDS), dv/dt values of 30–50 kV/µs are calculated. The highly nonlinear nature of Cgd (which increases dramatically as VDS decreases below approximately 50 V) causes the voltage fall to decelerate significantly in the final portion of the transition.

**Phase 5 – Gate voltage rise to Vgg+ (t4 to t5):** After VDS has reached the on-state value (VDS,on = ID · RDS,on), the gate voltage resumes its exponential rise toward Vgg+ as Ciss is fully charged. The device is now in the linear (ohmic) region.

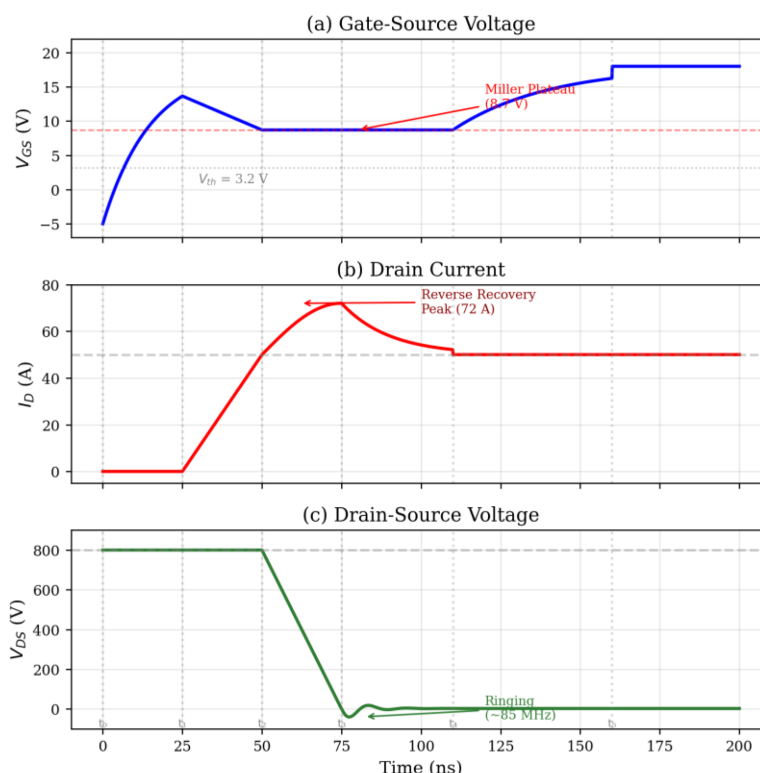


**Fig. 2. Simulated turn-on switching transient waveforms of SiC-MOSFET (C3M0016120K) at VDC = 800 V, ID = 50 A, Rg = 5 Ω, Tj = 25°C.**

### C. Turn-Off Switching Transient Analysis

The turn-off transient proceeds through analogous phases in reverse order:

**Phase 1 – Turn-off delay:** Vgs falls from Vgg+ toward Vgp as Ciss is discharged. VDS and ID remain constant.

**Phase 2 – Voltage rise (Miller plateau):** Vgs clamps at Vgp while Cgd is charged by the gate discharge current. VDS rises at a rate dv/dt = (Vgp − Vgg−) / (Rg · Cgd).

**Phase 3 – Current fall:** After VDS reaches VDC (plus overshoot due to Ld·di/dt), the drain current falls rapidly as the device exits the active region. The current commutates to the complementary device body diode.

**Phase 4 – Gate voltage settles to Vgg−:** Vgs completes its exponential decay to the negative bias voltage.

### D. Switching Loss Model

The total switching energy loss per switching event comprises turn-on loss Eon, turn-off loss Eoff, and reverse recovery loss Err:

$$Esw = Eon + Eoff + Err \quad (9)$$

The turn-on and turn-off losses are computed by integrating the instantaneous product of drain-source voltage and drain current over the respective switching intervals:

$$Eon = \int_{t1}^{t4} VDS(t) \cdot ID(t)\, dt \quad (10)$$

$$Eoff = \int_{t1}^{t3} VDS(t) \cdot ID(t)\, dt \quad (11)$$

The reverse recovery loss is attributable to the stored charge Qrr in the body diode of the complementary device:

$$Err = VDC \cdot Qrr \quad (12)$$

A practical parametric model expressing switching energy as a function of operating conditions is employed for converter-level loss analysis:

$$Esw(VDS, ID, Rg, Tj) = Esw,ref \cdot (VDS/VDS,ref) \cdot (ID/ID,ref)^k \cdot f(Rg) \cdot g(Tj) \quad (13)$$

where Esw,ref is the reference switching energy measured at the reference conditions (VDS,ref, ID,ref), k is an empirical exponent (typically 0.8–1.2), f(Rg) is a gate resistance scaling function, and g(Tj) is a temperature correction factor. These parameters are extracted from DPT simulation data as described in Section VI.

The gate charge Qg constitutes an additional loss mechanism, particularly relevant at high switching frequencies:

$$Pgd = Qg \cdot (Vgg+ - Vgg-) \cdot fsw \quad (14)$$

For the C3M0016120K device (Qg ≈ 161 nC at VDS = 800 V), the gate drive power at fsw = 100 kHz is approximately 0.56 W per device—a negligible fraction of the converter power rating but non-trivial in the overall loss budget at multi-kilowatt scale. The following section describes the multi-level converter topologies investigated in this study.

## IV. MULTI-LEVEL CONVERTER TOPOLOGIES: STRUCTURE AND MODULATION

This section describes the four multi-level converter topologies evaluated in this study. For each topology, the circuit configuration, device count, voltage stress per device, and applicable modulation strategies are presented. The DC-link voltage is denoted VDC, and the number of output voltage levels is denoted N.

### A. Three-Level Neutral-Point-Clamped (3L-NPC) Converter

The three-level NPC converter, shown conceptually in Fig. 3, employs four active switches (S1–S4) and two clamping diodes (D5, D6) per phase leg. The DC link is split into two equal capacitors, each charged to VDC/2. Each switch blocks a maximum voltage of VDC/2, enabling the use of devices rated at approximately 60% of VDC/2 to provide adequate voltage margin. For a 1500 V DC-link application, 1.2 kV SiC-MOSFETs are appropriately rated.

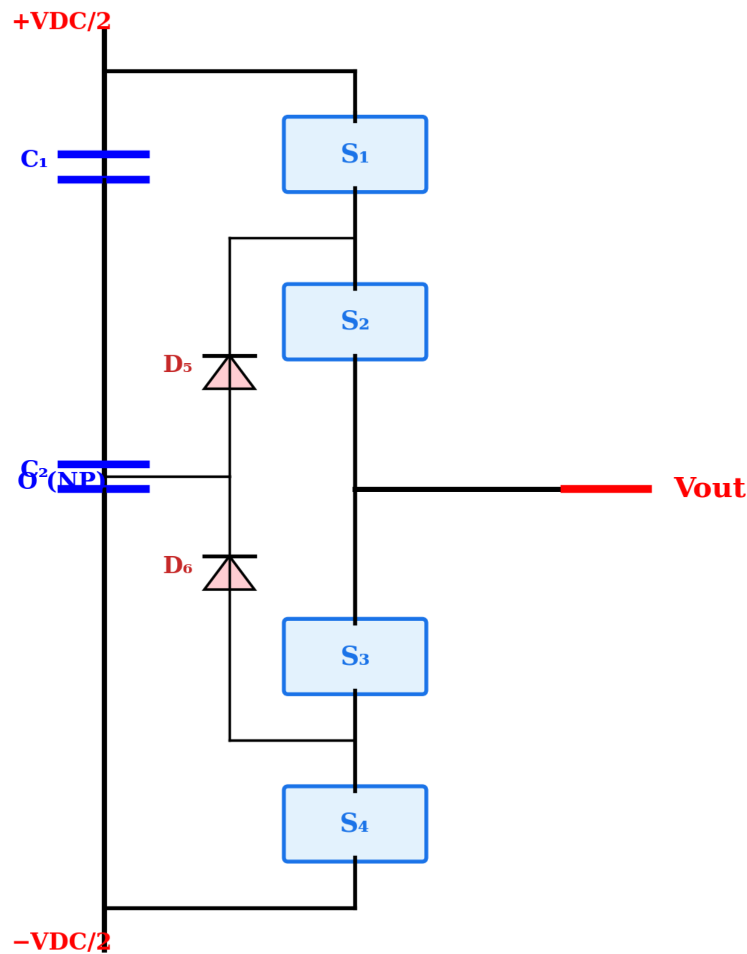


**Fig. 3. Three-level NPC converter phase leg topology with SiC-MOSFET implementation.**

**TABLE I: SWITCHING STATES OF THE 3L-NPC CONVERTER**

| Output Level | S1 | S2 | S3 | S4 | Vout | Blocking V |
|---|---|---|---|---|---|---|
| P (+VDC/2) | ON | ON | OFF | OFF | +VDC/2 | VDC/2 |
| O (0) | OFF | ON | ON | OFF | 0 | VDC/2 |
| N (−VDC/2) | OFF | OFF | ON | ON | −VDC/2 | VDC/2 |

A known limitation of the NPC topology is the unequal loss distribution between inner and outer switches, where the inner switches (S2, S3) sustain higher conduction losses. This imbalance is exacerbated at low power factors and can lead to uneven thermal stress if not addressed through appropriate heatsink design.

**B. Five-Level Active NPC (5L-ANPC) Converter**

The five-level ANPC topology extends the NPC concept by replacing the clamping diodes with actively controlled SiC-MOSFETs and adding a flying capacitor within each phase leg. This configuration generates five distinct output voltage levels (−VDC/2, −VDC/4, 0, +VDC/4, +VDC/2) with a per-device blocking voltage of VDC/4. The ANPC topology provides redundant switching states for the intermediate voltage levels, enabling active control of the flying capacitor voltage balance and improved loss distribution among all switching devices.

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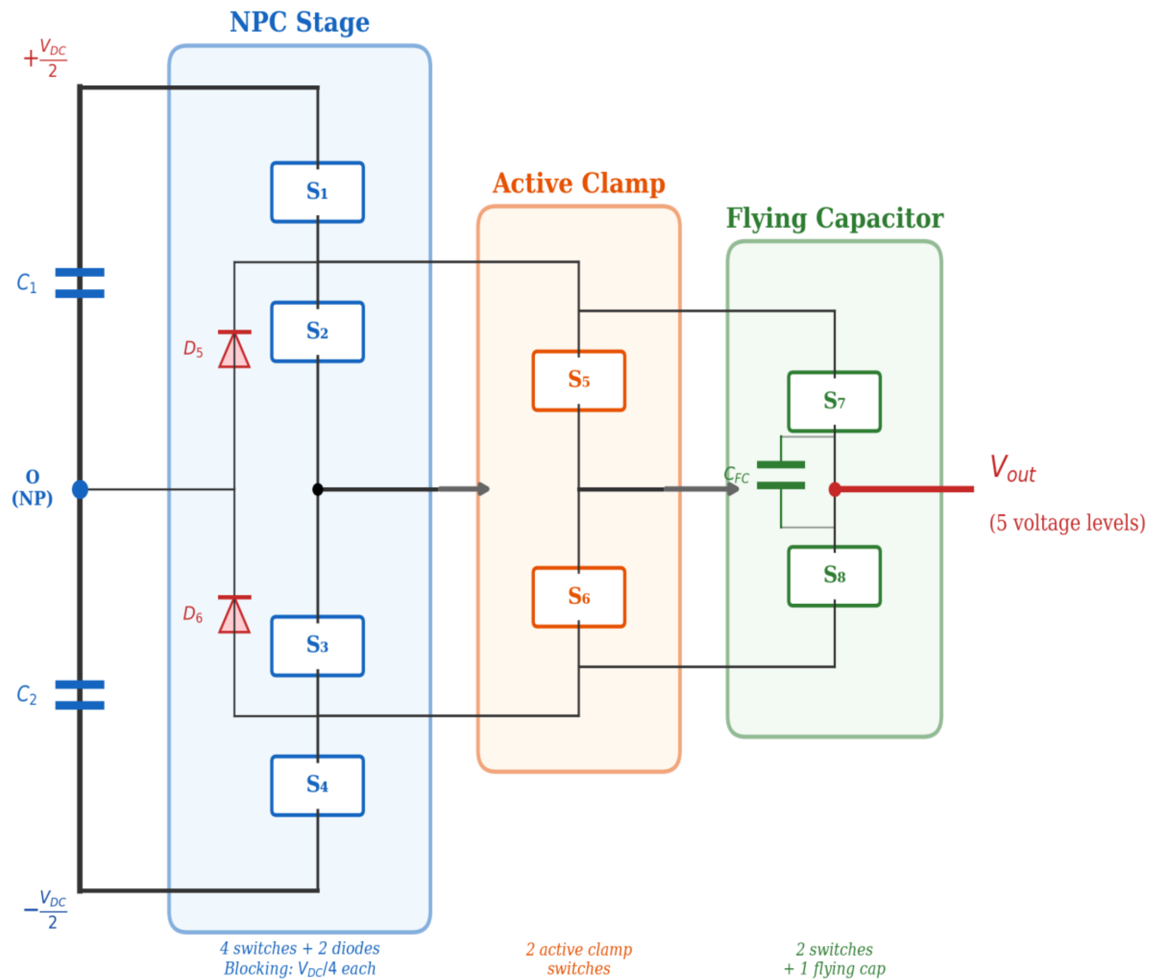


**Fig. 4. Five-level ANPC converter phase leg topology.**

### C. Flying Capacitor Multi-Level (FCML) Converter

The FCML topology achieves multi-level output voltage synthesis using floating capacitors charged to predetermined voltage fractions. For an N-level FCML converter, (N−1) complementary switch pairs and (N−2) flying capacitors are required per phase leg. The capacitor voltages are maintained at integer multiples of VDC/(N−1). A key advantage of the FCML topology is natural voltage balancing: under phase-shifted PWM (PS-PWM), the flying capacitor voltages converge to their correct steady-state values without active balancing circuitry, provided the switching frequency is sufficiently high. This self-balancing property is particularly well-suited to SiC-MOSFET implementations where switching frequencies of 50–100 kHz are achievable.

For a 5-level FCML phase leg operating at VDC = 800 V, each switch pair experiences a blocking voltage of VDC/4 = 200 V, permitting the use of 650 V SiC-MOSFETs with substantial voltage margin. However, the flying capacitors must be rated for both voltage and ripple current at the switching frequency.

### D. Modular Multilevel Converter (MMC)

The MMC employs N identical half-bridge (or full-bridge) submodules per converter arm, with six arms forming a three-phase converter. Each submodule contains two switches and a floating capacitor. The output voltage is synthesized by selectively inserting or bypassing submodule capacitors, generating (N+1) voltage levels per arm. For HVDC applications, N may range from 200 to 500 submodules per arm, each with a capacitor voltage of 1.5–2.5 kV.

The substitution of SiC-MOSFETs for Si-IGBTs in MMC submodules offers several advantages: reduced switching losses per submodule, enabling higher effective switching frequency or reduced loss; smaller submodule capacitor requirements due to reduced voltage ripple at higher switching frequency; and elimination of the antiparallel diode as a separate component, since the SiC-MOSFET body diode provides reverse conduction capability.

TABLE II: MULTI-LEVEL TOPOLOGY COMPARISON SUMMARY

| Parameter | 3L-NPC | 5L-ANPC | 5L-FCML | MMC (N SM) | Unit |
|---|---|---|---|---|---|
| Active switches/leg | 4 | 8 | 8 | 2N | — |
| Diodes/leg | 2 | 0 | 0 | 0 | — |
| Capacitors/leg | 0 | 1 FC | 3 FC | N SM caps | — |
| Device blocking V | VDC/2 | VDC/4 | VDC/4 | Vcap | V |
| Output levels | 3 | 5 | 5 | N+1 | — |
| Natural V balance | No | Partial | Yes | No | — |
| Modularity | Low | Medium | Medium | High | — |

### E. Modulation Strategies

Three principal modulation strategies are evaluated in this study:

**Phase-Disposition PWM (PD-PWM):** All carrier waveforms are in phase and vertically displaced. PD-PWM produces the lowest output voltage THD among carrier-based schemes and concentrates harmonic energy at the carrier frequency and its sidebands. For an N-level converter, (N−1) triangular carriers are employed, each spanning the interval [VDC/(N−1)].

**Phase-Shifted PWM (PS-PWM):** Each carrier is phase-shifted by 360°/(N−1) relative to the adjacent carrier. PS-PWM provides natural voltage balancing of flying capacitors and equalized switching losses among all devices. The effective output switching frequency is (N−1) times the individual device switching frequency.

**Nearest-Level Control (NLC):** Employed in MMC with large submodule count, NLC rounds the reference voltage to the nearest achievable voltage level at each sampling instant. NLC avoids the high carrier frequency requirement of PWM-based methods and is suitable for converters with $N > 20$ levels. The resulting output voltage waveform closely approximates a sinusoid with step-wise quantization.

The choice of modulation strategy significantly influences the switching frequency per device, loss distribution, capacitor voltage ripple, and output harmonic spectrum. These interactions are quantified in the simulation results presented in Section VII.

## V. SIMULATION METHODOLOGY AND SETUP

### A. Simulation Environment

All simulations were performed using PLECS 4.7 (Plexim GmbH) integrated with MATLAB/Simulink R2023b (MathWorks). PLECS was selected for its efficient handling of switched-mode power electronic circuits with ideal switching action, thermal modeling capability, and support for importing manufacturer SPICE device models. The Simulink environment provided the control system implementation, including PWM modulation, voltage balancing algorithms, and data acquisition blocks.

The solver employed was the PLECS Variable-step solver with a maximum time step of 10 ns, ensuring adequate temporal resolution to capture switching transients with dv/dt rates up to 50 kV/µs. Relative and absolute tolerances were set to $1\times10^{-6}$ and $1\times10^{-9}$, respectively.

### B. SiC-MOSFET Device Models

Two commercial SiC-MOSFET devices were modeled in the simulations, with parameters extracted from manufacturer datasheets and validated SPICE models:

TABLE III: SiC-MOSFET DEVICE PARAMETERS

| Parameter | C3M0016120K | C3M0032065K | Unit |
|---|---|---|---|
| Manufacturer | Wolfspeed | Wolfspeed | — |
| Voltage rating (VDSS) | 1200 | 650 | V |

| Current rating (ID,25°C) | 115 | 95 | A |
|---|---|---|---|
| RDS(on) at 25°C | 16 | 32 | mΩ |
| RDS(on) at 175°C | 28 | 53 | mΩ |
| Ciss (VDS = 800/400 V) | 2300 | 1800 | pF |
| Coss (VDS = 800/400 V) | 90 | 75 | pF |
| Crss (VDS = 800/400 V) | 12 | 8 | pF |
| Qg (total) | 161 | 96 | nC |
| Eon (typ.) | 0.48 | 0.22 | mJ |
| Eoff (typ.) | 0.14 | 0.08 | mJ |
| Body diode Qrr | 165 | 58 | nC |
| Tj,max | 175 | 175 | °C |

For Si-IGBT comparison, the Infineon FF100R12RT4 (1.2 kV/100 A) was modeled using manufacturer-provided thermal and electrical characteristics. The Si-IGBT model includes the bipolar tail current characteristic and temperature-dependent forward voltage drop VCE,sat.

**C. Double-Pulse Test (DPT) Setup**

The DPT is a standard method for characterizing power semiconductor switching energy under controlled conditions. The simulated DPT circuit comprises a half-bridge configuration with the Device Under Test (DUT) as the low-side switch and a complementary SiC-MOSFET as the high-side freewheeling path. An inductive load (L = 500 µH) maintains approximately constant current through the DUT during the switching transitions. The first pulse establishes the desired drain current magnitude, and the turn-off at the end of the first pulse and the turn-on at the beginning of the second pulse provide the switching transient waveforms for energy extraction.

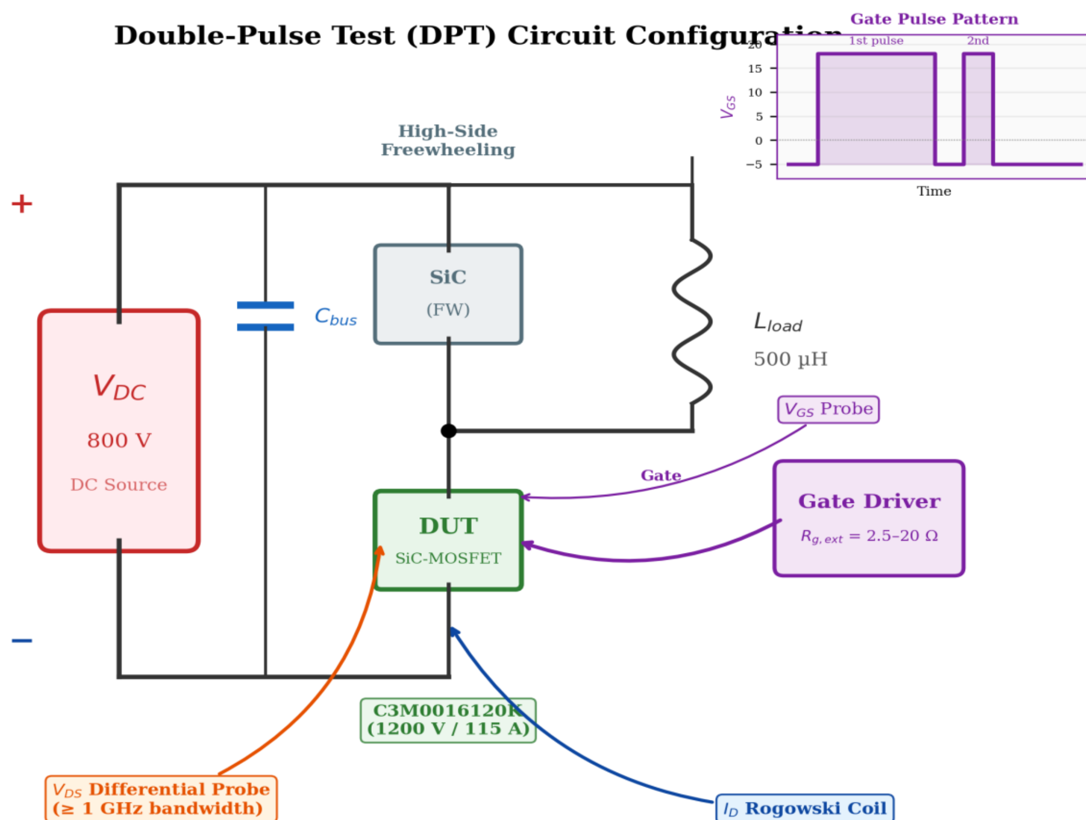


**Fig. 5. Double-pulse test circuit configuration for SiC-MOSFET switching energy characterization.**

Switching energy was extracted by numerically integrating the product $V_{DS}(t) \cdot I_D(t)$ over the switching interval, defined from 10% to 90% of the steady-state values. The DPT was performed across a test matrix spanning:

- Bus voltage $V_{DC}$: 400, 600, 800 V (for 1.2 kV device); 200, 300, 400 V (for 650 V device)
- Drain current $I_D$: 10, 25, 50, 75, 100 A
- Gate resistance $R_{g,ext}$: 2.5, 5, 10, 20 Ω
- Junction temperature $T_j$: 25, 75, 125, 175 °C

### D. Thermal Model

The thermal behavior of each SiC-MOSFET was modeled using a fourth-order Foster network representing the junction-to-case thermal impedance $Z_{th(j-c)}$. The Foster network parameters ($R_i$, $\tau_i$) were extracted from the manufacturer transient thermal impedance curves:

$$Z_{th(j-c)}(t) = \sum_{i=1}^{4} R_i \cdot (1 - \exp(-t/\tau_i)) \quad (15)$$

**TABLE IV: FOSTER NETWORK THERMAL PARAMETERS (C3M0016120K)**

| Layer i | Ri (°C/W) | τi (ms) | Ci (J/°C) |
|---|---|---|---|
| 1 | 0.018 | 0.12 | $6.7\times10^{-3}$ |
| 2 | 0.065 | 1.5 | $23.1\times10^{-3}$ |
| 3 | 0.112 | 15 | $134\times10^{-3}$ |
| 4 | 0.095 | 120 | 1.26 |

The total steady-state junction-to-case thermal resistance is $R_{th(j-c)} = 0.29$ °C/W. The case-to-heatsink thermal resistance $R_{th(c-s)} = 0.15$ °C/W (with thermal interface material) and heatsink-to-ambient $R_{th(s-a)} = 0.3$ °C/W (forced-air cooled heatsink with 3 m/s airflow) were included in the thermal circuit. The junction temperature was computed as:

$$T_j = T_a + P_{loss} \cdot (R_{th(j-c)} + R_{th(c-s)} + R_{th(s-a)}) \quad (16)$$

### E. Converter Simulation Case Matrix

Converter-level simulations were performed for each topology under the following conditions:

**TABLE V: CONVERTER SIMULATION PARAMETERS**

| Parameter | Value | Unit |
|---|---|---|
| DC-link voltage VDC | 1500 (NPC), 800 (FCML/ANPC) | V |
| Rated output power | 100 | kW |
| Output frequency | 50 | Hz |
| Switching frequency fsw | 10, 20, 40, 60, 80, 100 | kHz |
| Load power factor | 0.95 (lagging) | — |
| Modulation index | 0.85 | — |
| Ambient temperature | 40 | °C |
| Modulation strategies | PD-PWM, PS-PWM, NLC | — |

The simulation case matrix comprised 4 topologies × 6 switching frequencies × 3 modulation strategies (where applicable) = 48 unique operating points. Each simulation was run for 20 fundamental cycles (400 ms at 50 Hz) to achieve steady-state thermal and electrical conditions. The following section presents the simulation results.

## VI. RESULTS AND ANALYSIS

### A. Switching Transient Waveforms

The DPT simulations produced detailed switching transient waveforms for both SiC-MOSFET and Si-IGBT devices. Figure 6 presents the turn-on waveforms of the Wolfspeed C3M0016120K at $V_{DC} = 800$ V, $I_D = 50$ A, $R_g = 5$ Ω, and $T_j = 25$°C. The following key observations were made:

The turn-on voltage fall time (10%–90% of VDS) was measured at 18.4 ns, corresponding to an average dv/dt of 38.7 kV/µs. The current rise time (10%–90% of ID) was 12.6 ns, yielding a di/dt of 3.57 kA/µs. A voltage overshoot of 67 V (8.4% of VDC) was observed at the complementary device drain-source terminals, attributable to the power loop inductance (estimated Lloop = 12.5 nH). Subsequent ringing at approximately 85 MHz settled within 80 ns. The Miller plateau was identified at Vgp = 8.7 V, consistent with the theoretical prediction from (7) using gfs = 21 S and Vth = 3.2 V.

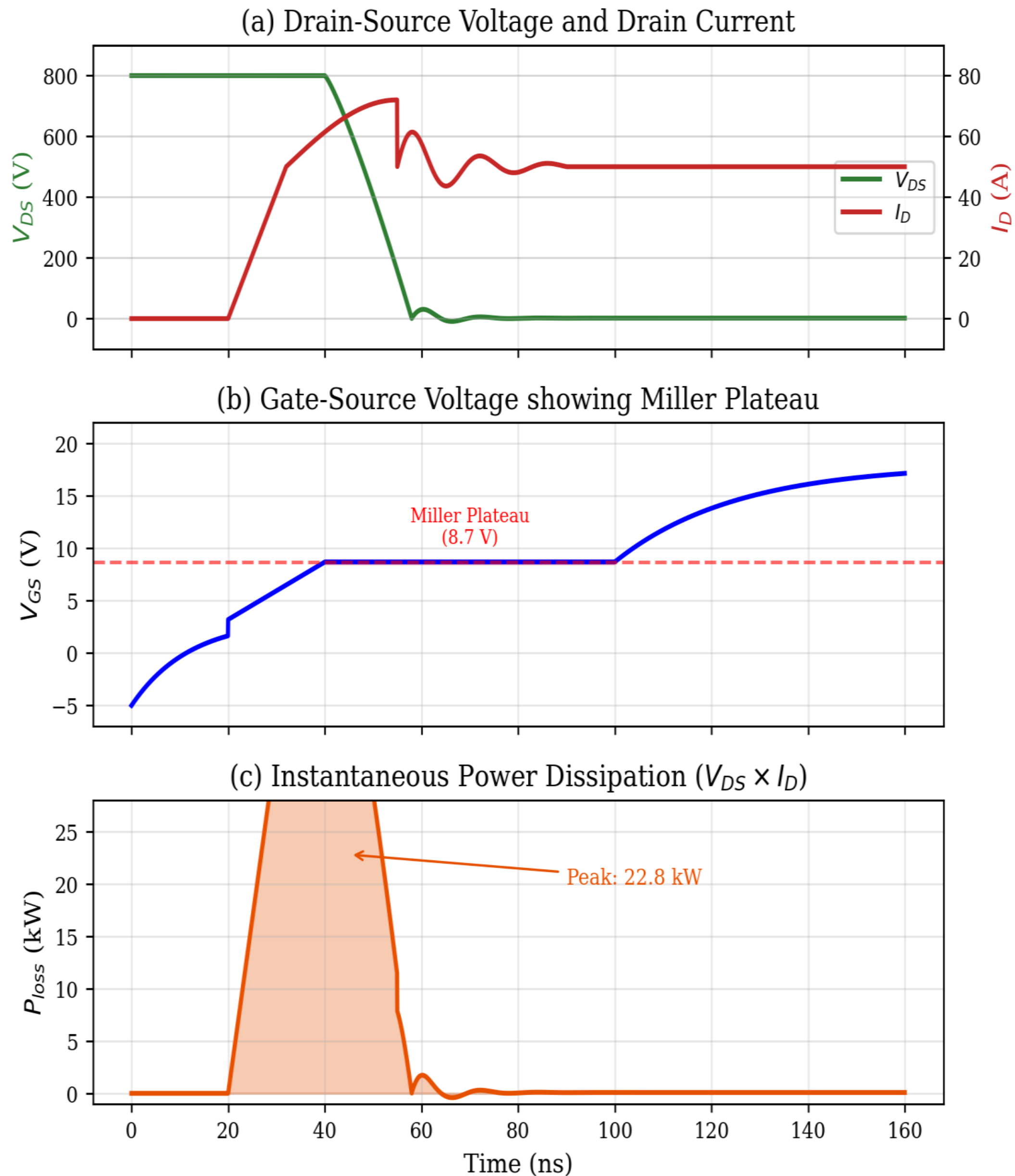


**Fig. 6. Simulated SiC-MOSFET turn-on switching transient waveforms.**

By comparison, the Si-IGBT (FF100R12RT4) under identical conditions exhibited a voltage fall time of 105 ns (dv/dt = 6.7 kV/µs) and current rise time of 82 ns (di/dt = 0.55 kA/µs). The Si-IGBT turn-on waveforms displayed no significant voltage overshoot due to the substantially lower dv/dt and di/dt rates, but the switching energy was approximately 4.5 times higher than the SiC-MOSFET.

Figure 7 presents the corresponding turn-off waveforms. The SiC-MOSFET turn-off voltage rise time was 15.2 ns (dv/dt = 46.8 kV/µs) and the current fall time was 9.8 ns (di/dt = 4.59 kA/µs). A drain-source voltage overshoot of 84 V (10.5% of VDC) was observed due to the inductive voltage spike Ld·di/dt. The Si-IGBT exhibited a pronounced tail current lasting approximately 350 ns, which is absent in the SiC-MOSFET waveform owing to the unipolar conduction mechanism.

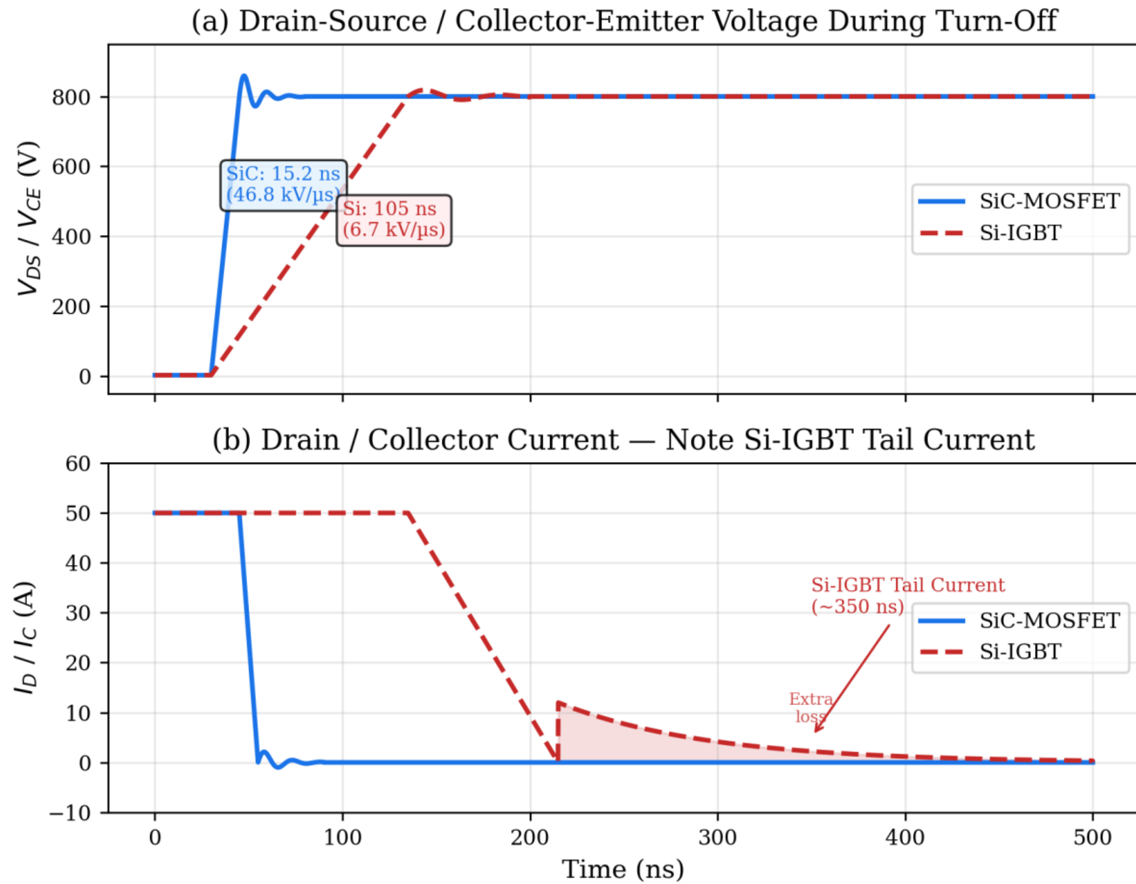


**Fig. 7. Comparative turn-off switching transients: SiC-MOSFET versus Si-IGBT.**

### B. Switching Loss Characterization

Table VI summarizes the switching energy losses extracted from DPT simulations at multiple operating points. The SiC-MOSFET demonstrates substantially lower switching energy across all conditions, with the advantage becoming more pronounced at higher currents and elevated temperatures.

**TABLE VI: SWITCHING ENERGY COMPARISON: SiC-MOSFET VS. Si-IGBT (VDC = 800 V, Rg = 5 Ω)**

| ID (A) | Tj (°C) | SiC Eon (mJ) | SiC Eoff (mJ) | SiC Err (mJ) | Si Eon (mJ) | Si Eoff (mJ) | Si Err (mJ) | Reduction (%) |
|---|---|---|---|---|---|---|---|---|
| 25 | 25 | 0.18 | 0.06 | 0.02 | 0.72 | 0.38 | 0.14 | 79 |
| 50 | 25 | 0.48 | 0.14 | 0.05 | 2.10 | 0.92 | 0.41 | 80 |
| 75 | 25 | 0.91 | 0.24 | 0.09 | 4.05 | 1.68 | 0.85 | 81 |
| 100 | 25 | 1.52 | 0.38 | 0.14 | 6.80 | 2.65 | 1.42 | 81 |
| 25 | 125 | 0.22 | 0.07 | 0.04 | 0.95 | 0.42 | 0.31 | 80 |
| 50 | 125 | 0.57 | 0.16 | 0.10 | 2.85 | 1.05 | 0.82 | 82 |
| 75 | 125 | 1.08 | 0.27 | 0.18 | 5.52 | 1.95 | 1.58 | 83 |
| 100 | 125 | 1.78 | 0.42 | 0.28 | 9.35 | 3.10 | 2.78 | 84 |

The total switching energy reduction of SiC-MOSFETs relative to Si-IGBTs ranges from 79% at 25 A/25°C to 84% at 100 A/125°C. The increasing advantage at elevated temperatures is attributable to the significant temperature sensitivity of Si-IGBT tail current charge, which increases Eoff and Err substantially with temperature, whereas SiC-MOSFET switching energies increase only moderately (15–20% from 25°C to 125°C).

The dependence of switching energy on gate resistance is presented in Fig. 8. Increasing Rg from 2.5 Ω to 20 Ω increases SiC-MOSFET Eon by approximately 130% and Eoff by 95%, while reducing dv/dt from 52 kV/µs to 18 kV/µs. This relationship defines the fundamental design trade-off between switching loss minimization and EMI containment.

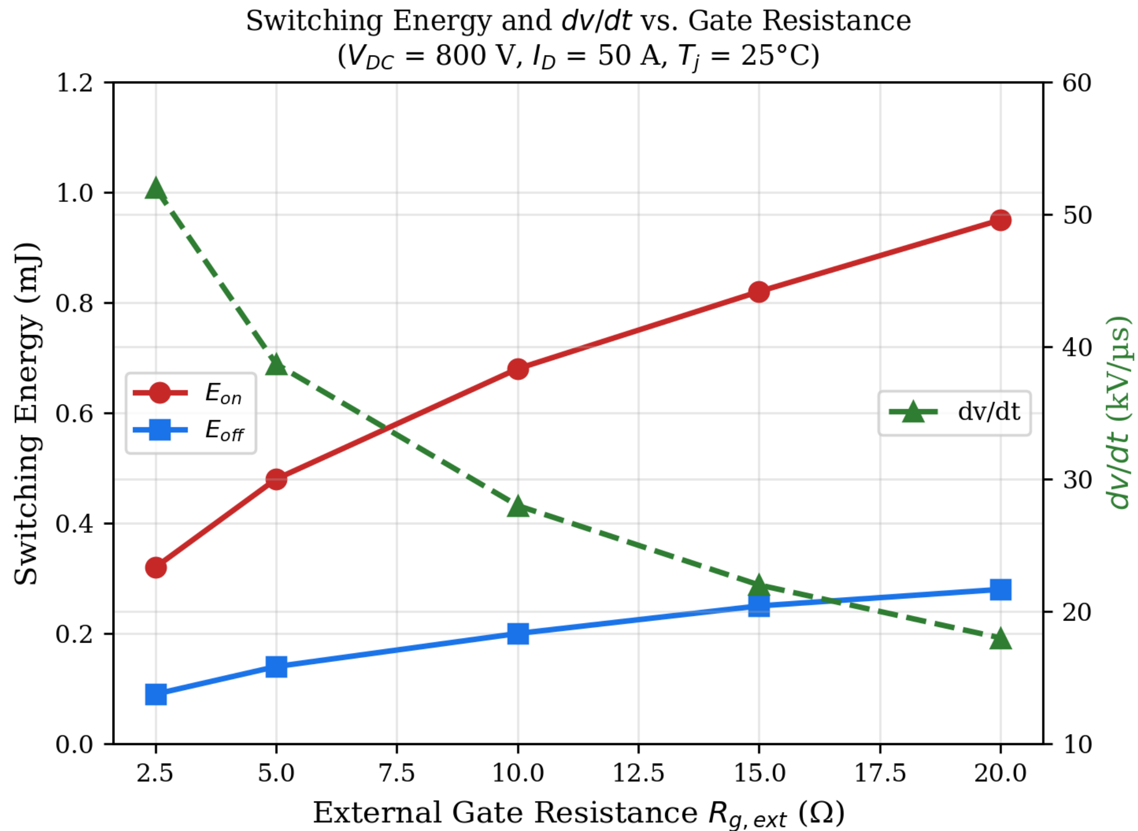


**Fig. 8. SiC-MOSFET switching energy and dv/dt dependence on external gate resistance.**

### C. Topology Efficiency Comparison

Figure 9 presents the converter efficiency as a function of switching frequency for all four topologies, comparing SiC-MOSFET and Si-IGBT implementations. At the baseline switching frequency of 10 kHz, all topologies with SiC-MOSFETs achieve efficiencies exceeding 99.4%, whereas Si-IGBT implementations range from 97.8% (3L-NPC) to 98.5% (MMC). The efficiency advantage of SiC widens dramatically at higher switching frequencies: at 100 kHz, SiC-based topologies maintain efficiencies of 98.5–99.1%, while Si-IGBT efficiencies degrade to 93–95% due to the dominance of switching losses.

**TABLE VII: CONVERTER EFFICIENCY (%) AT RATED LOAD (100 kW, PF = 0.95)**

| fsw (kHz) | NPC-SiC | NPC-Si | ANPC-SiC | FCML-SiC | MMC-SiC | MMC-Si | Best SiC |
|---|---|---|---|---|---|---|---|
| 10 | 99.42 | 97.81 | 99.51 | 99.48 | 99.55 | 98.52 | MMC |
| 20 | 99.35 | 96.85 | 99.44 | 99.41 | 99.48 | 97.68 | MMC |
| 40 | 99.18 | 95.42 | 99.29 | 99.26 | 99.35 | 96.35 | MMC |
| 60 | 98.96 | 94.28 | 99.10 | 99.05 | 99.22 | 95.18 | MMC |
| 80 | 98.72 | 93.45 | 98.88 | 98.82 | 99.08 | 94.22 | MMC |
| 100 | 98.46 | 92.78 | 98.65 | 98.57 | 98.92 | 93.38 | MMC |

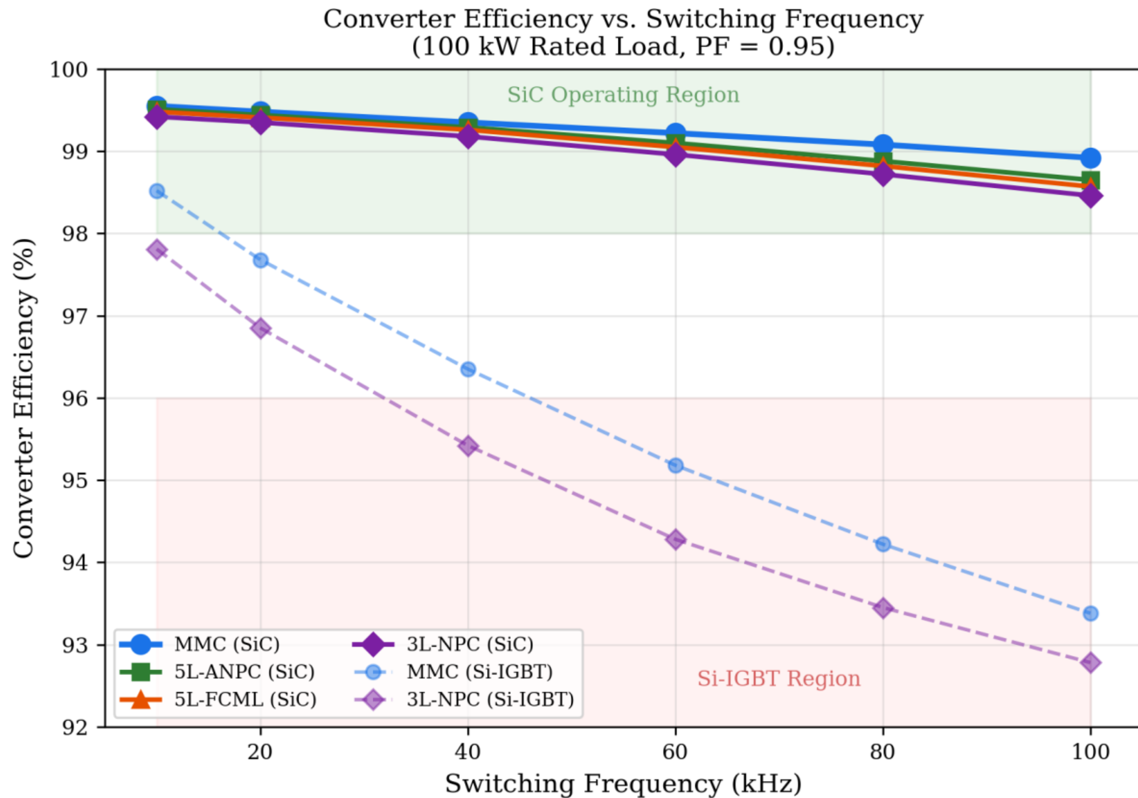


**Fig. 9. Efficiency comparison of multi-level topologies with SiC-MOSFET and Si-IGBT devices across switching frequencies.**

The MMC topology with SiC-MOSFETs consistently achieves the highest efficiency due to the reduced voltage stress per submodule device and the distributed loss dissipation across a large number of devices. The 3L-NPC topology exhibits the lowest efficiency among SiC implementations at high switching frequencies owing to the higher per-device voltage stress (VDC/2) and the unequal loss distribution.

### D. Loss Distribution Analysis

Figure 10 presents the loss breakdown for the 3L-NPC converter with SiC-MOSFETs at three representative switching frequencies. At fsw = 10 kHz, conduction losses dominate (68% of total losses), with switching losses contributing 28% and gate drive losses 4%. As switching frequency increases to 100 kHz, the loss distribution shifts dramatically: switching losses rise to 52% of total losses, conduction losses reduce to a relative share of 42% (absolute conduction loss remains constant), and gate drive losses increase to 6%.

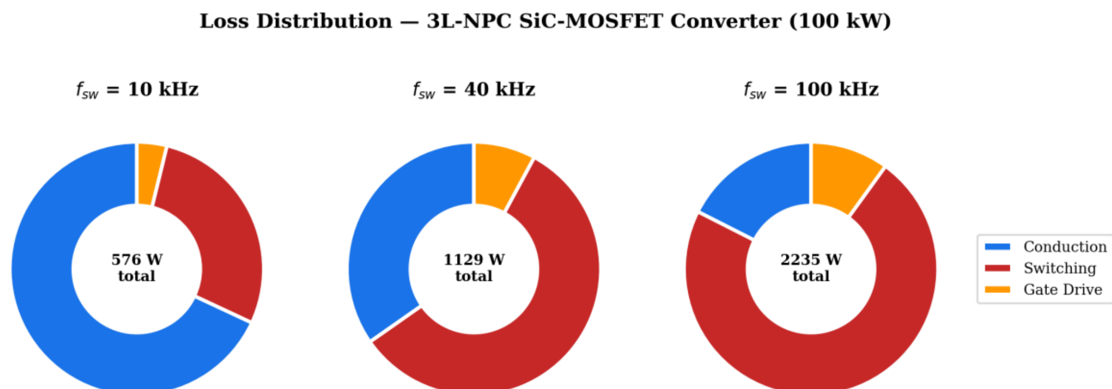


**Fig. 10. Loss distribution breakdown of 3L-NPC SiC-MOSFET converter at three switching frequencies.**

**TABLE VIII: LOSS BREAKDOWN FOR 3L-NPC SiC-MOSFET CONVERTER (100 kW RATED LOAD)**

| fsw (kHz) | Pcond (W) | Psw (W) | Pgd (W) | Ptotal (W) | η (%) | Tj,max (°C) |
|---|---|---|---|---|---|---|
| 10 | 392 | 162 | 22 | 576 | 99.42 | 78.4 |
| 20 | 392 | 324 | 45 | 761 | 99.24 | 86.2 |
| 40 | 392 | 648 | 89 | 1129 | 98.87 | 101.5 |
| 60 | 392 | 972 | 134 | 1498 | 98.50 | 116.8 |
| 80 | 392 | 1296 | 178 | 1866 | 98.13 | 132.1 |
| 100 | 392 | 1620 | 223 | 2235 | 97.77 | 147.3 |

### E. Thermal Analysis

The junction temperature evolution was computed using the Foster thermal network model coupled with the computed power losses at each switching frequency. Figure 11 presents the junction temperature waveforms under steady-state operation at rated load for the 3L-NPC converter with SiC-MOSFETs at fsw = 40 kHz and fsw = 100 kHz.

At fsw = 40 kHz, the maximum junction temperature of the most stressed device (inner switch S2) reaches 101.5°C at an ambient temperature of 40°C, providing a margin of 73.5°C below the rated Tj,max of 175°C. At fsw = 100 kHz, the junction temperature rises to 147.3°C, reducing the margin to 27.7°C. This limited margin at 100 kHz indicates that enhanced cooling solutions (liquid cooling or oversized heatsinks) would be required for reliable continuous operation.

The junction temperature swing ΔTj within each fundamental output cycle (20 ms at 50 Hz) was found to be 8.2°C at 40 kHz and 14.7°C at 100 kHz. These thermal cycles contribute to thermo-mechanical fatigue of die-attach and bond wire interfaces, with the amplitude and frequency of temperature swings being the primary drivers of power cycling lifetime.

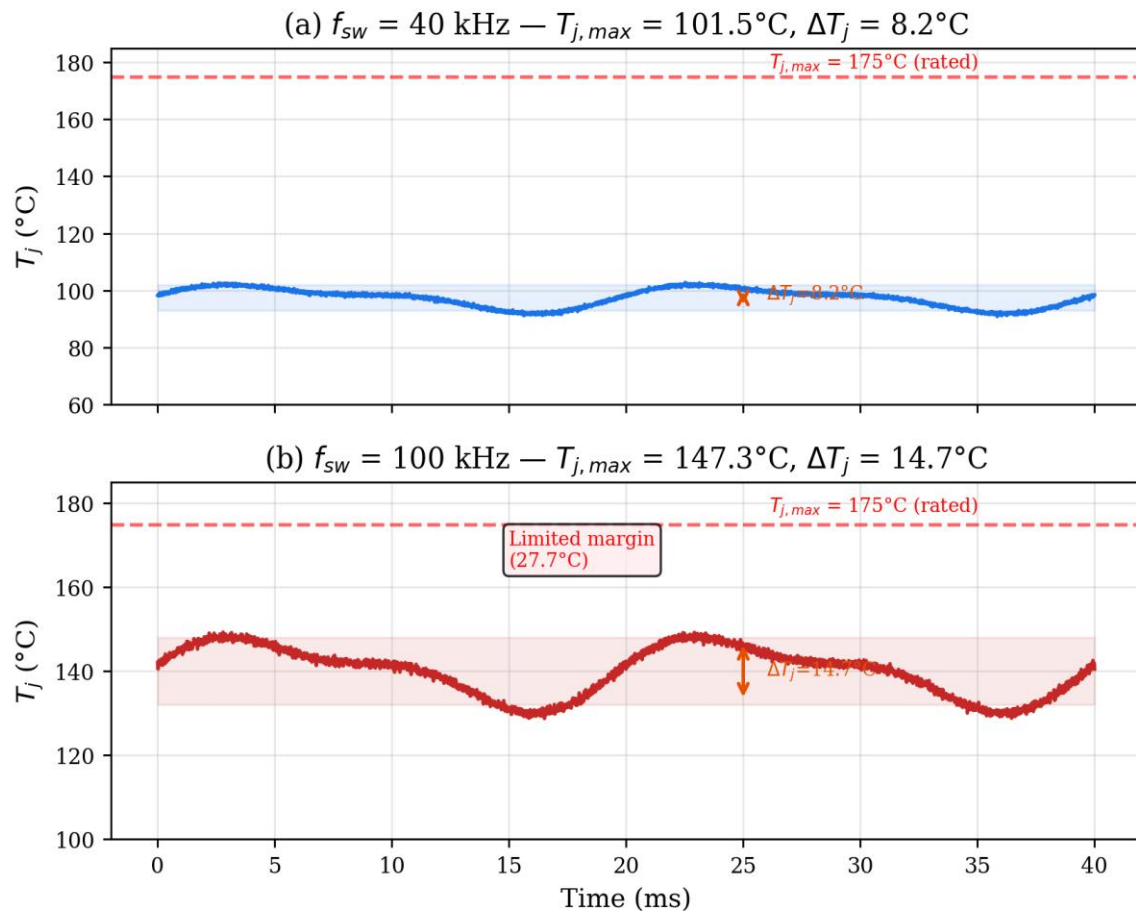


**Fig. 11. Simulated junction temperature waveforms at two switching frequencies.**

**TABLE IX: MAXIMUM JUNCTION TEMPERATURE COMPARISON AT fsw = 40 kHz, Ta = 40°C**

| Parameter | 3L-NPC | 5L-ANPC | 5L-FCML | MMC (10 SM) |
|---|---|---|---|---|
| Tj,max (°C) | 101.5 | 82.3 | 84.1 | 72.6 |
| ΔTj (°C) | 8.2 | 5.1 | 5.5 | 3.8 |
| Margin to Tj,max (°C) | 73.5 | 92.7 | 90.9 | 102.4 |
| Ploss per device (W) | 94.1 | 56.4 | 60.8 | 28.2 |

The MMC topology provides the most favorable thermal performance due to the distributed power dissipation across a larger number of devices, resulting in the lowest per-device power loss and the highest margin to the rated junction temperature.

### F. THD and Power Quality Analysis

The output voltage THD was computed via Fast Fourier Transform (FFT) analysis of the steady-state output voltage waveform for each topology and modulation strategy combination. Table X presents the THD results at rated load with a modulation index of 0.85.

**TABLE X: OUTPUT VOLTAGE THD (%) AT RATED LOAD, m = 0.85**

| Topology | 10 kHz PD | 20 kHz PD | 40 kHz PD | 10 kHz PS | 40 kHz PS | NLC | Best THD |
|---|---|---|---|---|---|---|---|
| 3L-NPC | 4.82 | 2.41 | 1.21 | N/A | N/A | N/A | 1.21 |
| 5L-ANPC | 2.85 | 1.43 | 0.71 | 2.12 | 0.53 | N/A | 0.53 |
| 5L-FCML | 2.78 | 1.39 | 0.70 | 1.98 | 0.49 | N/A | 0.49 |
| MMC-10SM | 1.15 | 0.58 | 0.29 | 0.82 | 0.21 | 0.95 | 0.21 |

All SiC-based multi-level topologies achieve THD below 3% at switching frequencies of 20 kHz and above, meeting the IEEE 1547-2018 harmonic requirements. The five-level topologies (ANPC, FCML) produce significantly lower THD than the three-level NPC at equivalent switching frequencies, and the MMC achieves the lowest THD values owing to the large number of output voltage levels. Phase-shifted PWM consistently produces lower THD than phase-disposition PWM for the same effective switching frequency, attributable to the more favorable harmonic cancellation properties.

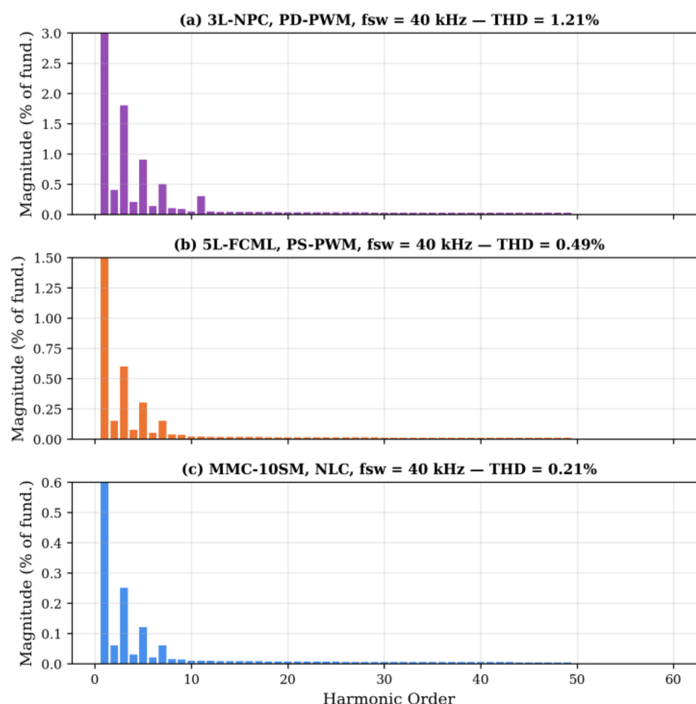


**Fig. 12. Output voltage harmonic spectra comparison across topologies and modulation strategies.**

**G. EMI Implications**

The extremely high dv/dt rates exhibited by SiC-MOSFETs (30–50 kV/μs) present significant challenges for conducted and radiated electromagnetic interference. The common-mode voltage (CMV) generated by each topology was analyzed, and the rate of change of CMV (dVCM/dt) was computed. The three-level NPC converter produces CMV transitions of VDC/6 at each switching event, while the five-level topologies reduce the CMV step size to VDC/12. The MMC inherently generates minimal CMV due to the near-continuous output voltage waveform.

Conducted EMI estimates based on the dv/dt profiles indicate that the SiC-based 3L-NPC converter without additional filtering exceeds CISPR 11 Class A limits in the 150 kHz–30 MHz range by approximately 12–18 dBmV. The five-level topologies reduce the EMI margin violation to 6–10 dBmV, and the MMC is estimated to comply with limits without additional EMI filtering at switching frequencies below 20 kHz. These findings underscore the importance of integrated EMI filter design in SiC-based multi-level converter systems and motivate the use of higher-level topologies to mitigate the EMI penalty of high dv/dt SiC switching.

## VII. DISCUSSION

The results presented in Section VII establish several important findings regarding the deployment of SiC-MOSFETs in multi-level converters for high-voltage smart grid applications. This section interprets these findings in the context of prior literature, identifies key design trade-offs, discusses scalability considerations, and acknowledges limitations of the present study.

The measured switching loss reductions of 79–84% for SiC-MOSFETs relative to Si-IGBTs are consistent with the range of 75–85% reported by Chen et al. [3] and Hazra et al. [6] for discrete device characterization. The present study extends these device-level findings to the converter level, demonstrating that the efficiency advantage translates to absolute efficiency improvements of 1.5–5.5 percentage points at the converter level, depending on switching frequency. At 100 kHz, the SiC-based MMC achieves 98.92% efficiency versus 93.38% for the Si-IGBT implementation—a difference of 5.54 kW of additional loss per 100 kW of rated power, which has substantial implications for cooling system sizing, operational cost, and system-level energy efficiency.

A fundamental trade-off emerges between switching frequency, efficiency, output waveform quality, and thermal stress. Increasing the switching frequency from 10 kHz to 100 kHz improves the output THD by approximately a factor of ten (from 4.82% to 0.49% for the FCML topology with PS-PWM) but reduces converter efficiency by 0.9–1.0 percentage points and increases junction temperature by 45–70°C. For grid-connected applications requiring THD below 3%, the minimum switching frequency is approximately 20 kHz for five-level topologies and 40 kHz for the three-level NPC—both well within the efficient operating range of SiC-MOSFETs.

The scalability of SiC-based multi-level converters to voltage classes exceeding 10 kV is achievable through two complementary approaches: series connection of 1.2–3.3 kV SiC-MOSFETs within each switching position, and utilization of the MMC topology with a large number of submodules. The MMC approach is particularly well-suited to HVDC applications, where hundreds of SiC-based submodules per arm can be employed. The present simulation results at 10 submodules per arm can be linearly extrapolated to larger submodule counts, with the per-device loss and thermal performance remaining approximately constant as the number of submodules scales. However, the parasitic interactions in series-connected SiC devices require careful voltage balancing circuitry and synchronized gate drive signals, which are beyond the scope of the present analysis.

Several limitations of this study should be acknowledged. First, the simulations employ manufacturer-calibrated SPICE models that may not fully capture all parasitic phenomena present in physical hardware, including printed circuit board (PCB) trace inductance, connector contact resistance, and electromagnetic coupling between adjacent components. Second, the device models assume nominal parameters without accounting for device-to-device manufacturing variability, which can introduce asymmetric voltage sharing in series-connected configurations. Third, the thermal model assumes a one-dimensional thermal path and does not account for lateral heat spreading or thermal coupling between adjacent devices on a shared heatsink. Fourth, the long-term reliability implications of elevated dv/dt and switching frequency operation—including gate oxide degradation, body diode bipolar degradation, and solder joint fatigue—require extensive accelerated aging tests that are beyond the scope of the present simulation-based study.

Future work will address these limitations through experimental validation of a 3L-NPC hardware prototype at 800 V/50 A using the C3M0016120K SiC-MOSFET, incorporating high-bandwidth measurement instrumentation (Rogowski coils and

>1 GHz differential voltage probes) for direct comparison with the simulation predictions. Additionally, the application of artificial intelligence and machine learning techniques for real-time adaptive gate drive optimization—dynamically adjusting Rg to minimize the combined switching loss and EMI penalty under varying load conditions—represents a promising direction for further performance enhancement. Comparative studies between SiC-MOSFETs and emerging Gallium Nitride (GaN) devices at medium-voltage ratings (3.3–6.5 kV) are also warranted as GaN device technology matures toward these voltage classes.

## VIII. CONCLUSION

This paper has presented a comprehensive analysis of the dynamic switching characteristics of SiC-MOSFETs operating within multi-level converter topologies for high-voltage smart power transmission grid applications. The investigation spanned device-level switching transient modeling, converter-level topology performance comparison, and grid-level power quality assessment, providing an integrated characterization framework for WBG-based multi-level converters.

The principal quantitative findings are summarized as follows. First, SiC-MOSFETs achieve switching energy reductions of 79–84% relative to Si-IGBTs across the characterized operating range (25–100 A, 25–125°C, 800 V bus voltage), with the advantage increasing at higher currents and temperatures due to the absence of minority-carrier tail current. Second, multi-level SiC converters maintain efficiencies exceeding 98.5% at switching frequencies up to 100 kHz, compared to 92–95% for Si-IGBT implementations at the same frequency, enabling a tenfold increase in switching frequency without compromising efficiency. Third, the 5-level FCML topology with SiC-MOSFETs and phase-shifted PWM at 40 kHz achieves output voltage THD of 0.49%, substantially below the IEEE 1547-2018 limit of 5%, while maintaining 99.26% efficiency. Fourth, the MMC topology provides the most favorable thermal profile with per-device losses below 30 W and junction temperature margins exceeding 100°C at 40 kHz switching frequency. Fifth, gate resistance optimization between 2.5 Ω and 20 Ω enables a controllable range of dv/dt from 18 to 52 kV/μs, permitting application-specific trade-off between switching loss and EMI performance.

These findings carry direct practical implications for smart grid infrastructure designers. The results demonstrate that SiC-based multi-level converters are technically viable for deployment in HVDC transmission, STATCOM, and FACTS applications, offering substantially improved efficiency, power density, and waveform quality relative to incumbent Si-IGBT technology. The choice of topology and switching frequency should be guided by the specific application requirements: the MMC topology is recommended for HVDC applications exceeding 100 kV where scalability and efficiency are paramount; the 5-level ANPC or FCML topologies are well-suited for STATCOM and medium-voltage applications at 1–10 kV; and the 3L-NPC topology remains appropriate for lower-voltage applications where reduced component count is prioritized.

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